

<b>Notice of References Cited</b>	Application/Control No. 09/730,039	Applicant(s)/Patent Under Reexamination MOHAMED ET AL.	
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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
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**FOREIGN PATENT DOCUMENTS**

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Thomas M. Conte and Sumedh W. Sathaye. "Dynamic Rescheduling: A Technique for Object Code Compatibility in VLIW Architectures". Microarchitecture, 1995.
	V	Morteza Biglari-Abhari, Kamran Eshraghian, and Michael J. Liebelt. "Improving Binary Compatibility in VLIW Machines through Compiler Assisted Dynamic Rescheduling". Euromicro Conference, 2000. Proceedings of the 26 <sup>th</sup> , Volume: 1, 5-7 September 2000.
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,669,001	09-1997	Moreno, Jaime Humberto	717/149
	B	US-5,721,854	02-1998	Ebcioğlu et al.	712/203
	C	US-5,787,303	07-1998	Ishikawa, Tadashi	712/24
	D	US-5,848,288	12-1998	O'Connor, Dennis M.	712/24
	E	US-6,467,036	10-2002	Pechanek et al.	712/24
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
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	M	US-			

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Alberto Ferreira de Souza and Peter Rounce. "Dynamically Scheduling the Trace Produced During Program Execution into VLIW Instructions". Parallel and Distributed Processing, 1999. Proceedings, 12-16 April 1999.
	V	Michael Weiss, Zhixi Fang, C. Robert Morgan, and Peter Belmont. "Effective Dynamic Scheduling and Memory Management on Parallel Processing Systems". Computer Software and Applications Conference, 1989.
	W	Santoshkumar S. Pande, Dharma P. Agrawal, and Jon Mauney. "Palm: An Integrated Parallelism Enhancement Environment with Static-Dynamic Scheduling". System Sciences, 1992.
	X	B. Ramakrishna Rau. "Dynamically Scheduled VLIW Processors". Microarchitecture, 1993.

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.